Germanium Gate PhotoMOSFET Integrated to Silicon Photonics

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***Abstract*—This paper presents a novel germanium gated NMOS phototransistor integrated on a silicon photonics platform on silicon-on-insulator (SOI) substrate. The phototransistor is fabricated with a modified NMOS process flow, with germanium which is recrystallized using rapid melt growth during the source/drain activation anneal step. The resulting device, with 1-μm channel length, and 8-μm channel width, demonstrates a responsivity of over 18 A/W at 1550 nm with 583 nW of incident light. By increasing the incident power to 912 μW, the device operates at 2.5 GHz. Miniaturization is expected to improve both responsivity and speed in future devices.**

***Index Terms*—Phototransistors, photodetectors, optoelectronic devices, optical waveguide components, optical interconnections.**

I. Introduction

OPTICAL interconnects have shown tremendous promise in recent years for replacing electrical wires for both on-chip and off-chip communications. One primary challenge lies in developing low energy per bit receivers, of the order of 10 fJ/bit or less, for on chip communication [1]. Achieving this requires low capacitance photodiodes and tight integration with low capacitance receiver circuits. Many groups have worked on creating low capacitance (1–10 fF) photodiodes on waveguides [2]–[6]. There has also been a focus on integrating low-capacitance photodiodes through either wirebonding or monolithic integration with CMOS receiver circuitry [7]–[9].

The reduction in energy/bit comes from reducing the photodiode capacitance, and reducing the input capacitance of the transistor. With fF photodiodes, and sub-fF transistors, one begins to consider even the capacitance of the metal line connecting the photodiode to transistor with a capacitance of $\sim$0.2 fF/μm, almost independent of geometry [1]. This implies that 5 μm of wire connecting a 1-fF photodiode to the receiver circuitry effectively doubles the diode capacitance, while it takes only 1 μm of connecting wire to double the capacitance of a 200-aF photodiode. To solve this issue, the wire between photodiode and first transistor should be eliminated by integrating gain with the photodiode.

Several groups have recently demonstrated devices such as a normal incidence germanium photo bipolar junction transistor [10], a waveguide integrated germanium junction field-effect transistor [11], germanium avalanche photodiode [12], [13], and a normal incidence germanium gate MOSFET [14]. One issue with the previous photoMOSFET was that a polycrystalline germanium gate was deposited, which greatly inhibited performance. Crystalline germanium can be obtained on a gate oxide through wafer bonding [15], [16], epitaxial overgrowth [17], or rapid melt growth (RMG) [18].

In this paper we demonstrate a waveguide integrated germanium gate MOSFET, where RMG is used to create a monocrystalline gate. The NMOS device is fabricated using a self-aligned process on a 220-nm-thick SOI substrate that is compatible with standard silicon photonics integrated circuits. The source/drain activation anneal step melts and recrystallizes the germanium. A high responsivity of 18 A/W at 583 nW of 1550-nm light with only 8 μm of germanium along the waveguide indicates strong internal transistor gain. Due to a relatively long (1-μm) channel, the device has a 3-dB cutoff of 2.5 GHz, obtained with higher optical power. Standard scaling methodology is expected to provide for improvements in both the speed and responsivity of the device.

II. Phototransistor Design

A. Device Design

Shown in Fig. 1(b) is the schematic cross-section of the device. On the surface, the device is a traditional self-aligned NMOS with a silicon channel and a germanium gate. The silicon body layer is 220-nm thick, on 3 μm of buried oxide, and is also used as the silicon photonics layer. Coming out of the plane of the figure is the single mode silicon waveguide (500-nm wide) which tapers out to a grating coupler for optical input. The single mode waveguide abuts the transistor body as seen in the microscope image in Fig. 1(c). The light in the transistor body is then evanescently coupled into the germanium gate due to the higher refractive index of germanium [19]. Because the absorption length of germanium at 1550 nm is 5 μm, the gate widths were designed from 2–32 μm, with channel lengths between 0.25–2 μm. The confinement factor in the 1 $\times$ 8-μm germanium gate is 42.6% according to finite difference time domain (FDTD) mode calculations, which makes effective

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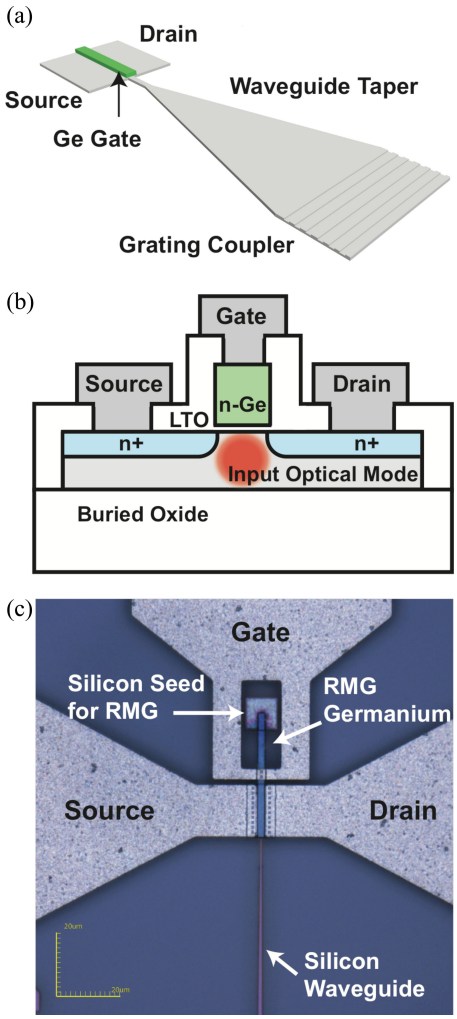

Fig. 1. (a) 3-D Schematic drawing of the photoMOSFET with integrated silicon photonics components. (b) Schematic cross-section of the photoMOSFET. (c) Optical micrograph of a completed photoMOSFET.

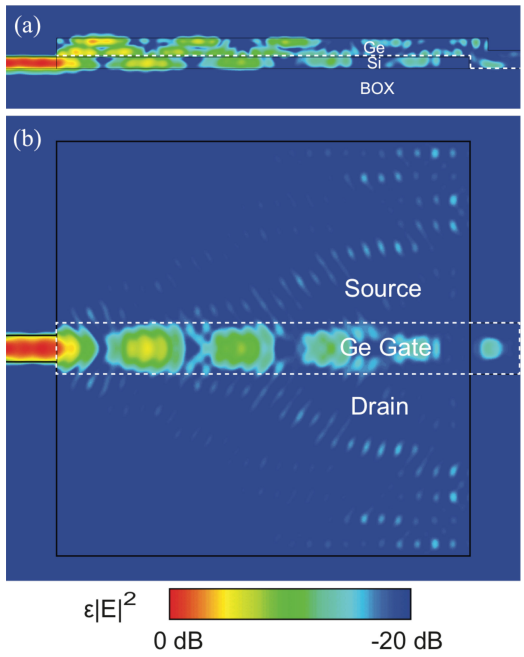

Fig. 2. (a) Slice through the middle of the gate, showing the energy distribution from FDTD between the germanium gate and silicon body along the interaction length. (b) Slice through the body of the transistor, showing energy confinement under the germanium gate in the silicon.

absorption length 852 cm^{-1}. For 8 μm of interaction length, in a single pass there should be 49% absorption in the germanium gate. An FDTD simulation estimates 55% absorption in the gate including back reflections. Fig. 2 shows the energy distribution both in the germanium gate and the underlying silicon from FDTD.

Because the bandgap of silicon is 1.1 eV and is indirect, the primary absorption in silicon at 1550 nm is due to free carrier absorption [20], which is minimized with a low p-type body doping of 10^{17} cm^{-3}. The silicon waveguide and all other silicon photonics structures have a much lower doping level of 10^{14} cm^{-3}, which will give low propagation loss. Additionally the mode quickly couples into the germanium gate, avoiding optical interaction with the much more heavily doped source/drain region in the silicon. Also seen in Fig. 1(c) is an electrically and optically isolated island of silicon near the transistor body which is used as the seed to crystallize the germanium during the RMG process [18]. Because the silicon body and crystal seed are separated laterally by the buried oxide layer, they are electrically isolated from each other.

The body doping was chosen to be uniform for simplicity with a single boron implant giving a channel doping of 10^{17} cm^{-3}, which would give a maximum depletion width of 105 nm [21]. The source and drain doping were chosen to give 10^{20}-cm^{-3} n-doping for ohmic contact, while simultaneously n-doping the germanium gate to 10^{18} cm^{-3}. A tailored screening oxide is deposited over the germanium to control the dose implanted into the germanium, allowing a lower doping concentration than the source and drain regions. A moderate doping concentration in germanium is desired to strike a balance between lowering the amount of depletion in the gate and having a lower recombination rate in the germanium for an optimal photoresponse.

B. *Theory of Operation*

The device is a photodiode with the cathode attached to the gate contact, and the anode attached to the gate oxide of the transistor. When not illuminated, the diode is reverse biased, and no current can flow through it, so there is a negligible voltage drop across the diode. In this case, the device functions much like a traditional long-channel MOSFET with a partially depleted gate, since the doping in the germanium gate is not very high.

When illuminated the germanium gate acts like an open circuit solar cell [21] and the photocurrent is balanced by recombination currents, resulting in a net photovoltage across the germanium. This voltage adds to the voltage applied by the gate contact, and the net voltage on the gate is higher. If we assume the germanium has a quantum efficiency, η, then the photovoltage, V_{photo}, can be described by (1) as a function of incident optical power. Here P_{inc} is the incident optical power on the

device at a frequency, ν, and I_s is the diode leakage current.

$$V_{\text{Photo}} = \frac{nkT}{q} ln\left(\frac{P_{\text{inc}}}{I_s}\frac{\eta q}{h\nu}\right). \quad (1)$$

Much like the subthreshold slope of a MOSFET, in this device, the additional gate voltage induced by light absorption follows a slope of 60 mV/decade of optical power, assuming Shockley–Read–Hall recombination dominates. The total voltage induced however, is also influenced by the quantum efficiency of the absorption and the internal diode leakage current. This condition will have an impact on ultimate device performance.

From this we can then calculate the photocurrent in the drain current, I_d, when the device is in saturation using the simple square law current equation. This gives both the bias current from the gate and drain voltages and the photocurrent in (2). Here it is assumed the transistor has gate length, L, gate width, W, with electron mobility, μ_n, gate oxide capacitance, C_{ox}, a threshold voltage, V_T, and an applied gate bias of V_g.

$$I_d = \frac{1}{2}\mu_n C_{\text{ox}}\frac{W}{L}\left(V_g + V_{\text{photo}} - V_T\right)^2. \quad (2)$$

It can be seen the photocurrent has a $\ln^2$ dependence on incident optical power as well as a dependence on gate voltage. Because the device is fundamentally an NMOSFET with a light modulated gate, one can choose which region to operate in depending on the requirements of the device. Much like an amplifier, this implies that in order to get a larger photoresponse from the device, a larger bias current is needed.

III. Fabrication and Characterization

A. Fabrication

Starting with a 220-nm SOI substrate with 3-μm buried oxide layer, a blanket boron implant was performed with a 10^{12} cm^{-2} dose at 30 keV with 7° tilt. The grating couplers were then formed with a 55-nm etch into the silicon (70-nm designed), followed by a full 220-nm silicon etch to form the waveguides. The full etch also isolates the crystal seed from the waveguides and transistor body. The wafers were then cleaned in piranha solution (1: 50 H_2O_2:H_2SO_4) followed by a 10:1 buffered HF (BHF) dip, to remove any organics and native oxide present. The wafers were then thermally oxidized in dry O_2 at 950 °C which grew a measured 17-nm oxide. The oxide was annealed in N_2 at 950 °C for 30 min.

A 10-μm seed hole was opened in the oxide with a dilute (50:1) HF solution after being defined lithographically. The resist was then immediately stripped with PRS-3000, cleaned in piranha solution followed by a 1 s 10:1 BHF dip, and placed under vacuum in a germanium LPCVD furnace. The gate oxide was measured to be 16 nm after the cleaning step before germanium deposition. To promote adhesion to the oxide, a 5-nm amorphous silicon layer was first deposited, followed by a 350-nm polycrystalline germanium layer. Finally a 20-nm LTO layer was deposited on top of the germanium to promote adhesion for subsequent photoresist steps. The thickness of this LTO also determines the total implant dose in the germanium.

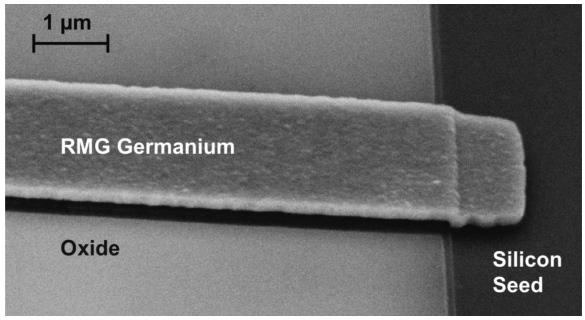

Fig. 3. SEM image of germanium strip after RMG with the oxide cap removed.

The germanium gate was then patterned and dry etched. A self-aligned phosphorus implant, with a dose of 10^{15} cm^{-2} at 20 keV with 7° tilt then formed the source, drain, and gate doping. 300 nm of LTO was deposited on the wafer, followed by a backside etch in HF and H_2O_2 at 50 °C to remove germanium from the backside of the wafer. Source/drain dopant activation was achieved with a rapid thermal anneal at 1000 °C for 1 s. This step also melted and recrystallized the germanium as in the RMG technique. Because the germanium is liquefied in this step, it is assumed the phosphorus dopants distribute uniformly throughout the gate.

Finally contact vias were formed in the oxide to the germanium and silicon by lithographic patterning and dry etching. The wafers then received a quick (10:1) HF dip and were immediately placed into the load-lock of an RF sputterer. 50 nm of Ti followed by 400 nm of $Al_{.98}Si_{.02}$ were sputtered onto the wafer. The metal layers were patterned and dry etched to form contact pads, and the wafer was then annealed in forming gas (H_2/N_2) at 450 °C for 30 min to form ohmic contacts.

B. Material Characterization

To first characterize the quality of the recrystallized germanium, an etch pit test was utilized on bare strips. The etching solution used was HF:HNO_3:CH_3COOH (1:3:10) [22]. Specifically the solution etches crystal dislocations and grain boundaries faster than the bulk crystal, resulting in pits and troughs. The etching was done for 30 s, which etched the defects to a size of 1 μm, large enough to be visible in an optical microscope. The defects were then counted on several strips of germanium, and an upper bound defect density of 10^6 cm^{-2} was calculated. Several 200-μm long germanium test strips showed the single crystal region extended over their entire length. It is thus reasonable to assert that the entire germanium gate on the photoMOSFET is single crystal. No transmission electron micrography analysis was performed, since other groups using RMG have performed extensive TEM imaging [4], [18], the RMG procedure used herein followed their methods, and the defect etch results generally agreed with their calculated defect densities. A scanning electron micrograph (SEM) showing the crystallized germanium can be seen in Fig. 3. A control sample with no exposed silicon for seeding was also prepared and the defect etch revealed polycrystalline germanium with grains on the order of 5 μm in size.

IV. Electrical and Optical Characteristics

A. Silicon Photonics

The passive silicon photonics components were first characterized on the chip. An angled single mode fiber was used to probe two back-to-back grating couplers, which also tapered down to single mode waveguides of different lengths. This is an optical analogue to the electrical transmission line measurement for contact resistance. The measured insertion loss for each grating and taper was 20 dB at 1550 nm, calculated by dividing the total back-to-back insertion loss by two. The high insertion loss was largely due to the gratings being slightly red-shifted due to an exposure error during the grating lithography step as well as high waveguide loss due to incomplete removal of germanium and aluminum during the dry etching steps. In all of the optical measurements of the devices, the grating and taper insertion loss is taken into account, such that the reported incident power is the actual power incident on the device from the single mode waveguide.

B. DC Electrical Characterization

The current and voltage characteristics were measured with an HP4145B parameter analyzer, with the chip in the dark, and then again illuminated with 1550 nm with an angled fiber through the grating couplers. The gate and drain voltages on each device were swept from 0 to 1.5 V, while the drain current was measured. For high incident power measurements, an erbium doped fiber amplifier was inserted after the laser source to compensate for the insertion loss of the gratings and tapers.

Several devices with gate lengths from 0.5 to 2 μm and gate widths from 2 to 32 μm were measured. Measured transconductance was in the range 8–141 mS/mm and threshold voltages were in the range 0.5–2.1 V. The results for a 1-μm channel length and 8-μm channel width device are shown in Fig. 4. When operated in saturation, the device shows that for a bias current of $\sim$150 μA, a 51-μA photocurrent is produced when illuminated with 468 μW, seen in Fig 4(a). The dark threshold voltage is 1.5 V from a linear extrapolation with a transconductance of 60 mS/mm. When 912 μW of 1550-nm light was incident on the device through the single mode waveguide, the extracted threshold was measured to be 1.285 V with the same transconductance, seen in Fig. 4(b).

The responsivity of the device can be extracted by dividing the photocurrent by the incident power, shown in Fig. 5, which shows responsivity as a function of gate and drain current. Much like transistor current, the photocurrent for a given input power is a function of the bias voltages. Higher gain can be obtained by increasing drain voltage, up to the point of saturation. Increasing the gate bias beyond the threshold voltage increases the photocurrent and responsivity. Because the device operates as a transistor with a photovoltage on the gate, the specific bias point of the transistor can be controlled by engineering the transistor itself, dictated by the specific output characteristic need.

The same transistor is then measured at several different optical input power levels. The photovoltage is extracted as a function of optical power, shown in Fig. 6. When fit with a linear

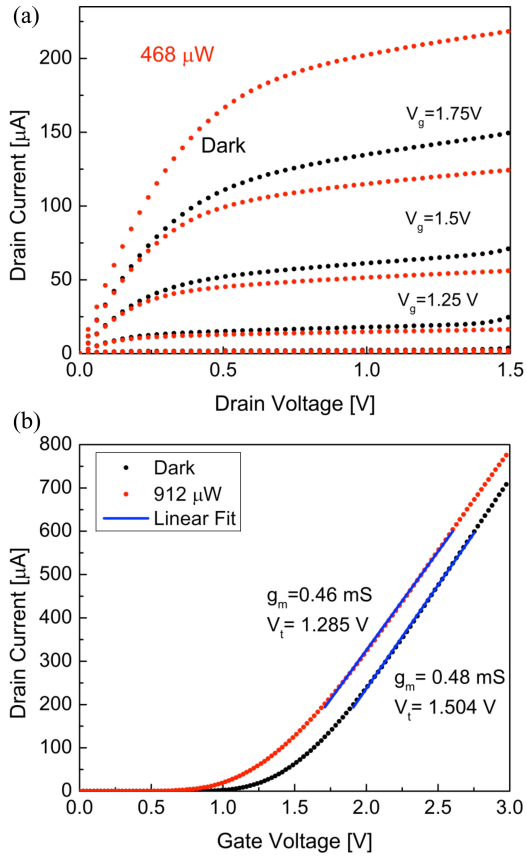

Fig. 4. (a) Drain current as a function of drain and gate voltage both in the dark and with 468 μW of illumination. (b) Drain current as a function of gate voltage at a drain voltage of 1 V. The transconductance and threshold voltage are extracted both in the dark and with 912 μW of illumination.

function, a 60-mV/dec relationship is measured, agreeing with the previous theory. While this may appear to be a fundamental limitation to device performance, it should be noted that the intercept of the line is dictated by the internal diode leakage current. For this device, the extrapolated diode leakage current is 240 nA. The device can be made more sensitive, to yield a larger photovoltage for a given input power level, by shrinking the gate area, or by reducing the recombination rate in the gate through improvement in material quality or by surface treatments [23].

The log relationship between the input power and the induced photovoltage implies that how the voltage is then converted into a current is important. When operating the transistor in saturation, the drain current has a square dependence on applied gate voltage, and the amplification of small optical signals will be larger than that of large optical signals. This can be seen in Fig. 5 where the responsivity for 0.5 μW of incident light is a very large 18 A/W, while at 0.5 mW of incident light the responsivity is closer to 0.15 A/W. In the subthreshold region of operation, the drain current has an exponential dependence on applied gate voltage, and there will be a linear dependence of drain current on optical power. However the overall output current is lower in subthreshold operation. When considering how to bias this device, one must consider device requirements such as linearity in optical response, output current, speed, and output impedance. Total photocurrent output in all regions of

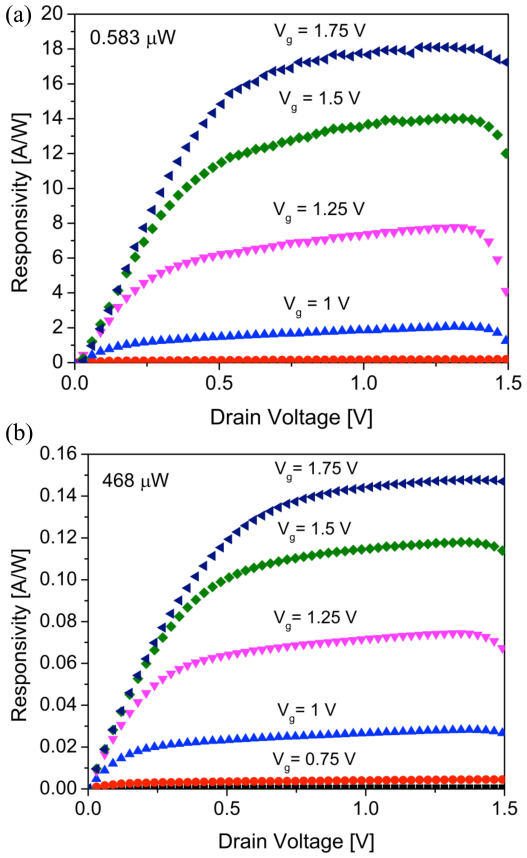

Fig. 5. (a) Measured responsivity with 0.583 μW of incident power. (b) Measured responsivity with 468 μW of incident power.

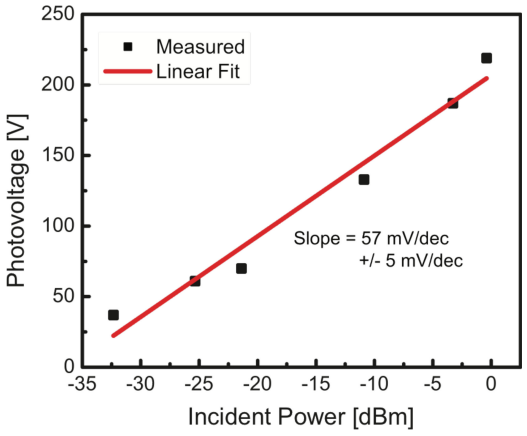

Fig. 6. Extracted photovoltage as a function of incident power.

operation can be increased by decreasing the germanium diode area and by increasing the transistor transconductance.

V. High Speed Operation and Future Scaling

A. High Speed Operation

The high speed light response was measured with an Agilent 110-GHz network analyzer. The source and drain were contacted through a ground-signal-ground 50-GHz probe, with 1.2 V of drain bias applied through a bias-T. The drain current signal was put directly into port 2 of the analyzer. The gate was biased to 1.5 V with a dc probe. Port 1 of the analyzer drove a 20-GHz intensity modulator, which modulated the 1550-nm light input into the transistor. The frequency response was calibrated with a commercial 34-GHz photodiode. The frequency response was measured with an input power of 912 μW shown in Fig. 7. The spectrum was fit with a single pole function, indicating a 3-dB frequency of 2.5 GHz. A 2.5-GHz 3-dB frequency was also measured at 1.37 mW of input power, which was the maximum available given the limitations of the laser source and erbium doped fiber amplifier, and also with 468 μW of input power. Below 468 μW of input power, the signal to noise ratio of the measurement became too low to accurately measure the 3-dB frequency.

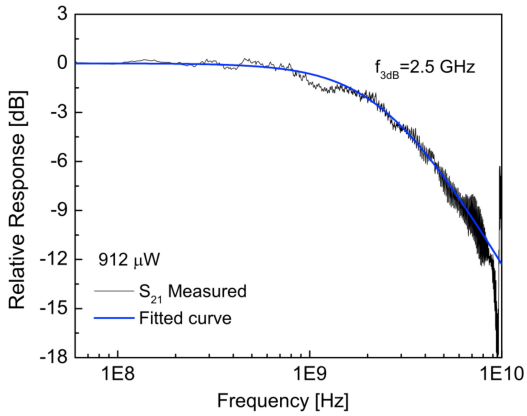

Fig. 7. Relative response to optical excitation as a function of frequency.

$$f_T = \frac{g_m}{2\pi(C_{\rm ox} + C_{\rm par})} \tag{3}$$

where $C_{\rm ox}$ is the gate oxide capacitance and $C_{\rm par}$ is the parasitic gate capacitance.

We can calculate the cut-off frequency of the transistor using (3) [21], and use the measured transconductance, $g_m = 0.46$ mS, while assuming a gate capacitance from the patterned dimensions of 1×8 μm, and the measured 16-nm gate oxide, which gives a calculated gate oxide capacitance of 17.3 fF. With no parasitics this gives a 4.3-GHz cut-off frequency. In this particular device, the crystal seed was not trimmed from the gate, leaving over 25 μm of excess germanium, which should have about 5 fF of additional capacitance. Also because only a single deep source/drain implant was used, there is likely considerable gate-drain overlap capacitance in the device. Taking all of these into account, would then indicate that the measured 3-dB frequency of the device is comparable to the natural cut-off frequency of the transistor. This indicates that by improving the doping profiles, and scaling the dimensions of the gate, the phototransistor should be able to operate at much higher speeds.

The other major component to the response time of this device is the relaxation time of the germanium gate. When the incident light is turned-off, the minority carriers present in the germanium must recombine to reduce the photovoltage present in the gate. This recombination lifetime is also directly correlated to the amount of photovoltage generated for a given amount of incidence light, since in steady state the generation and recombination rates balance. In this device, since the measured cut-off

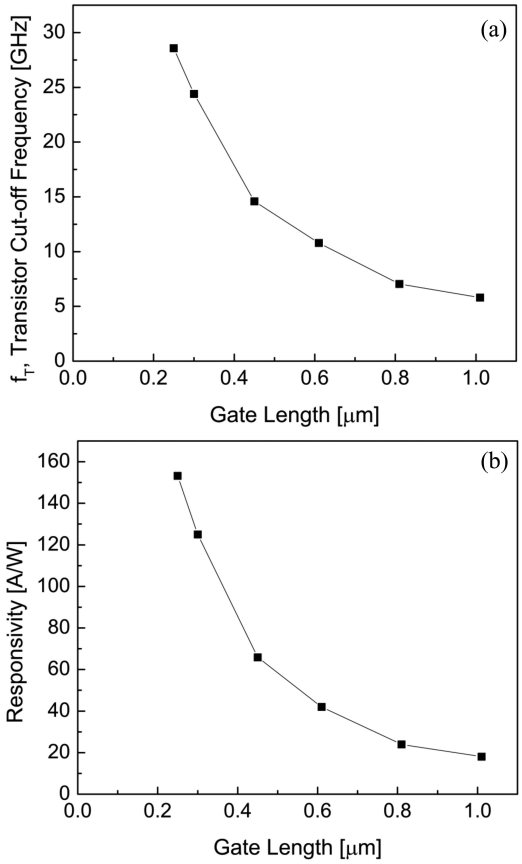

Fig. 8. (a) Simulated cut-off frequency as a function of gate length with scaling. (b) Simulated responsivity as a function of gate length with scaling.

frequency is similar to the calculated theoretical cut-off for just the transistor, it is assumed the recombination lifetime in the germanium is not a limiting factor. However if the transistor is scaled to increase the bandwidth, a more detailed investigation of the germanium recombination lifetime will be needed to determine possible speed limitations from that effect.

B. Future Scaling

To investigate the potential benefits of scaling this device, we have run device simulations in Sentaurus. The specific process used in this paper was simulated to generate the device in the simulator, followed by electrical and optical simulations. To simulate optical excitation, a constant carrier generation model was used. First the simulation results were calibrated against the measured data. Constant field scaling was applied [21], where the gate oxide was thinned by the scale factor, the ion implant energy decreased by the scale factor, the gate length reduced by the scale factor, and the body implant dose increased by the scale factor. All other conditions remained the same, and the applied gate bias remained 1.5 V and the drain bias remained 1 V. The per-unit gate width transconductance is extracted from each simulation, and from the geometrical dimensions, the gate oxide capacitance is calculated. Using (3), the cut-off frequency is calculated, and plotted against gate length in Fig. 8(a). The calculation assumes no additional parasitic capacitances on the gate. Additionally, the simulation of optical generation was calibrated with the measured data, and under the same conditions, the responsivity is plotted as a function of the scaled gate length in Fig. 8(b). In the simulation it is assumed that scaling does not affect the quantum efficiency of absorption, since a constant carrier generation model is used. In general this will not be true, since narrower gates will alter the confinement of light within the germanium, affecting the needed volume for absorption, and ultimately the total absorbed power. For scaling to very short gate lengths, additional optical engineering will be needed to ensure good absorption in small gate volumes.

It can be seen that by shrinking to 250-nm gate length, with 4-nm gate oxide, the cut-off frequency would reach 28 GHz. Following this same trend, a 100-nm gate length would be needed to reach 40 GHz, which is well within the capability of the state-of-the-art (22-nm node) technology. However one large assumption is that the relaxation time of the germanium gate diode is much faster than the transistor cut-off time. This time depends largely on recombination lifetime within the germanium, and will depend largely on material quality, and doping concentration in the germanium. As the gate shrinks in volume, surface recombination will become a bigger factor, and the dimensions of the gate will also affect the germanium recombination lifetime.

In addition to a speed boost from shrinking the gate, the responsivity of the device should increase as well, which comes from two factors. One is that the induced photovoltage will increase with reduced gate area, since diode leakage current in the gate will reduce with the gate area. Additionally, a shorter gate will increase transconductance, meaning that for a given photovoltage, a larger drain current will be produced. When simulated, the 250-nm gate length device shows 150-A/W responsivity.

VI. Conclusion

In this paper we demonstrate a germanium gate photoMOSFET, which is highly sensitive to light at 1550 nm. The unique aspects of the design are the rapid melt grown germanium gate, which gives a single crystal material on the gate oxide with a low diode leakage current. The second unique aspect is the direct integration of the device with silicon photonics, utilizing silicon waveguides with the natural transistor gate geometry for efficient light absorption. With a 1×8 μm gate area device, the responsivity was measured to be as high as 18 A/W and was found to operate at speeds upward of 2.5 GHz. With traditional MOSFET scaling, the device will improve both in speed and sensitivity, yielding a viable potential photodiode/pre-amp receiver for low-energy optical communication.

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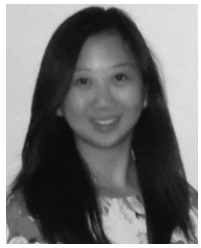

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